comp.lang.vhdl

Frequently Asked Questions And Answers (Part 3): Products & Services

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Preliminary Remarks

This is a monthly posting to comp.lang.vhdl containing information products and services for VHDL (commercial and public domain) Please send additional information directly to the editor:

edwin@ds.e-technik.uni-dortmund.de (Edwin Naroska)

Corrections and suggestions are appreciated. Thanks for all corrections.

There are three other regular postings: part 1 lists general information on VHDL, part 2 lists books on VHDL, part 4 contains descriptions for a number of terms and phrases used to define VHDL.

This product list is never up to date it seems - please help to update it. This list is without any guarantee to be complete or correct. It is included to enable contacts to vendors. It does not contain version, quality or price information. (Please accept, that actually this information changes to fast -too much work to keep such information up to date, but if there is a volunteer willing to take this part...:-). If some kind of judgment is included (’specialist’ for example) it’s not my personal opinion but a remark from the vendor himself.

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FAQ comp.lang.vhdl (part 3): Products & Services

1. Special Stuff, Shareware, Public Domain

For free demo or introductory versions of various software packages (mostly for developing FPGAs, CPLDs, and PLDs) see http://www.optimagic.com/lowcost.shtml. Additional free software packages covering various aspects of hardware design may be found at http://collector.hscs.wmin.ac.uk/.

1.1 VHDL scanner/parser

For additional VHDL parser search the "The Hamburg VHDL archive" at http://tech-www.informatik.uni-hamburg.de/vhdl/vhdl.html.

A VHDL Parser/Generator written in Prolog

Description: A Public Domain VHDL Parser/Generator written in Prolog is available via anonymous FTP from the Microelectronics Center of North Carolina (MCNC.ORG). Look for vhdl.tar.Z in /pub. For a more up-to-date version of this software (including bug fixes, a graphical editor and logic synthesis modules), contact Peter Reintjes at Quintus Corporation: pbr@quintus.com or pbr@deerfeld.ingr.com (I work for DASIX now!).

Contact: Peter Reintjes, Email: pbr@quintus.com
A revised Version can now be found at

- *URL:* ftp://ftp.cs.wright.edu/pub/vhdl/
  Files: VHDL93.tar.Z and README

A VHDL-93 Parser written in SWI_Prolog

Description: A VHDL-93 Parser written in SWI_Prolog (Version 2.7.14) conforming to the IEEE 1076-1993 Standard of VHDL is available from the Wright State University. An experimental VHDL-93 Design Description Browser written in Tcl/TK (Version 7.5/4.1) by Laura DeBrock is also included. The parser is a revised version of the VHDL-87 parser in Quintus Prolog by Peter Reintjes.

Contact: Krishnaprasad Thirunarayan (Prasad), Email: tkprasad@cs.wright.edu, phone: (513)-873-5109
URL: ftp://ftp.cs.wright.edu/pub/vhdl/
Files: VHDL93_SWI_2.7.14.tar.gz and README_SWI_2.7.14

A VHDL-1076.1 (AMS) Parser/Pretty-Printer written in SWI_Prolog

Description: This distribution contains a VHDL-1076.1 parser and pretty-printer in SWI-Prolog (and an experimental Graphical User Interface written in Java). It evolved from the VHDL-87 Parser in Quintus Prolog written by Peter B. Reintjes.

Contact: Krishnaprasad Thirunarayan (Prasad), Email: tkprasad@cs.wright.edu, phone: (513)-873-5109
URL: http://www.cs.wright.edu/people/faculty/tkprasad

A Lex and yacc based VHDL parser

Description: Another parser based on lex an yacc can be found at the University of Dortmund (Germany) .It can parse and analyze arbitrary VHDL code and convert it into

an abstract syntax graph. It handles many of the more challenging semantic issues of VHDL like type checking and overload resolution.

URL: http://www-dt.e-technik.uni-dortmund.de/~mvo/vaul/

A VHDL grammar and frontend based on the compiler toolbox CCTB

Description: A VHDL grammar and frontend based on the compiler toolbox CCTB of GMD of the University of Karlsruhe. Note that the status of both topics is quite different: the grammar is a (more or less) finished product, the frontend certainly not. A VHDL grammar based on lex and yacc, manually derived from the CCTB version is also available.

The tools are available from

- Grammar
  URL: ftp://ftp.cs.utwente.nl/pub/src/VHDL/Grammar
  File: vhdl-lexyacc.1.4.tar.Z
- Frontend
  URL: ftp://ftp.cs.utwente.nl/pub/src/VHDL/FrontEnd

VHDLParser and VHDLTree

Description: The first free pure Java VHDL Parser plus graphical structure viewer for VHDL design files. Contributed by Andreas Dangberg.

Contact: Email: sprudel@c-lab.de
URL: http://home.wtal.de/software-solutions/vhdl-parser

VHDL-AMS Parser by Christoph Grimm

Description: The parser covers the complete IEEE 1076 - Standard including the extensions proposed as IEEE 1076.1. I implemented it using the JavaCC Compiler-Compiler from SUN. Currently, only syntax check works.

Contact: Email: grimm@ti.informatik.uni-frankfurt.de
URL: http://www.ti.informatik.uni-frankfurt.de/grimm/hybrid.html

SUAVE (SAVANT and University of Adelaide VHDL Extensions) Parser

Description: The SUAVE project is a joint effort between the University of Cincinnati and the University of Adelaide to design and evaluate object-oriented extensions for the hardware description language VHDL. Currently, a parser/analyzer is available.

Contact: Email: phil.wilsey@uc.edu
URL: http://www.ececs.uc.edu/~paw/suave

1.2 VHDL Compilers, Synthesis Tools

VDT and INSPIRE

Description: VDT (VHDL Developer's Toolkit) and INSPIRE (a VHDL Simulation Environment with **IN**cremental Analysis/Elaboration, **SP**ecialized Functions, and **I**ncremental Waveform **RE**generation) is a free (?) VHDL simulation system supporting a subset of the IEEE 1076 VHDL standard. Binaries are available for Linux and Sun and Windows.

URL: http://poppy.snu.ac.kr/vdt-ivsim/vhdlsim.html
URL: ftp://poppy.snu.ac.kr/pub/vhdl/

ALLIANCE 3.0

Description: ALLIANCE 3.0 is a complete set of CAD tools for teaching Digital CMOS VLSI Design in Universities. It includes VHDL compiler and simulator, logic synthesis tools, automatic place and route, etc... ALLIANCE is the result of a ten years effort at University Pierre et Marie Curie (PARIS VI, France). ALLIANCE allows VLSI designers to

- capture and simulate VHDL behavioral views.
- capture and validate structural views.
- produce physical layout.
- verify layout (DRC).
- check layout against structural (logical/extracted) and behavioral (formal proof) views.

The complete ALLIANCE CAD Framework is available by anonymous FTP. For more info see ALLIANCE.README at the distribution sites.

URL: http://www-asim.lip6.fr/alliance/

AMICAL

Description: AMICAL is an Interactive Architectural Synthesis Tool based on VHDL developed at the system level synthesis group of TIMA Laboratory at INPG, Grenoble, France. AMICAL starts with a functional specification given in VHDL, it performs scheduling, allocation and generates an architecture composed of a data-path and a controller that may feed existing synthesis tools acting at the logic and register transfer levels. AMICAL uses a powerful scheduler and accepts a quite large VHDL subset (multiple waits, nested loops, exits, procedures, functions...). The present version produces a VHDL description that can be accepted by Synopsys. AMICAL is organized as an interactive environment, it provides several facilities for architecture analysis (statistics, evaluation, links between the VHDL behaviour and the resulting architecture...). The response time of AMICAL is short enough to make it an interactive system. AMICAL is available free of Charge. The present version has already been distributed to several experimental centers. The present version runs on SPARC station under SUNOS. Two versions of the graphical interface exists: Openwindow, Suntools. The distribution include:

- The AMICAL software.
- A Tutorial
- A user’s Manual
- A beginner Session
- Synthesis exercices (6 Hours)

The distribution does not include the VHDL analyser. The present version makes use of the VHDL Analyser of CLSI. A new version based on LVS, the VHDL compiler from LEDA, will be available soon. In case you have no the right VHDL analyser we added, the distribution may include the compiled and scheduled version of all the examples. Then you can use AMICAL with a fixed scheduling in order to perform interactive synthesis. Of course this is useful only for practicing with AMICAL or for Demonstration.

URL: http://tima-cmp.imag.fr/tima/sls/amical/amical.html

Electric

Description: Electric is a sophisticated electrical CAD system that can handle many forms of circuit design, including Custom IC layout (ASICs), Schematic drawing, Hardware description language specifications, and Electro-mechanical hybrid layout. The VHDL system can generate VHDL from a layout, and can compile structural VHDL to netlists of various format. These netlists can then be simulated with the built-in simulator, turned into layout with the silicon compiler, or saved to disk for use in external simulators.

URL: http://www.gnu.org/software/electric/electric.html
URL: http://www.staticfreesoft.com/
A Macintosh build of the Electric VLSI design tools is available from
URL: http://members.aol.com/djohn4077/html/electric.html

SAVANT

Description: The SAVANT project is an effort by University of Cincinnati's Computer Architecture Design Lab to build an extensible, object-oriented intermediate form (IIR) for the hardware description language VHDL. The project produced a suite of software to analyze VHDL, build the IIR, and output C++ suitable for execution with the TyVIS VHDL simulation kernel. Further, the SAVANT analyzer has been designed to easily allow the insertion of new back-ends into the tool. The software developed under the SAVANT project is freely available. Users may modify, distribute, and use the software contained in the SAVANT software package under the terms of the "GNU LIBRARY GENERAL PUBLIC LICENSE" version 2, June 1991.

URL: http://www.ececs.uc.edu/~paw/savant
URL: ftp://ftp.ececs.uc.edu/pub/users/dmartin/
URL: http://www.cliftonlabs.com/savant/download/

Free VHDL-AMS to C++ for Simulink translator

Description: Main AMS constructions and statements are supported, with focus on AMS quantities, vectors and fast execution (possibly in real time):

- entity, architecture
- default port and generic values, mapping actual ports/ generics
- REAL, REAL_VECTOR(size) indexed from 0, vector literals, easy-to-add other vector types
- first order ODE for both REAL and REAL_VECTOR via 'DOT
- simple_simultaneous_statement assumes as assignment
- simultaneous_if_statement, generate_statement - FOR only
- component_instantiation_statement
- vector'HIGH, vector'LOW
- 'ABOVE defined for REAL, other attributes easy to add
- relational, algebraic and logical operators
- initialization and conditional BREAK

Connectivity to Simulink:

- as S-Function - compiled shared library
- vector ports

- easy simulation control, use of other Simulink modules
- several fixed/variable-step ODE solvers

Translator is made using rapid development JavaCC container technology. Complicated features as aggregates of record types, subtype ranges etc. can't be implemented. Other executable statements are easy to add. Semantical checking is left for C++ compiler. No signals or processes can be translated.

URL: http://paneris.org/~peterk/vhdlams/

1.3 Editors

VHDL support for GNU Emacs or XEmacs

Description: GNU Emacs (http://www.gnu.org/software/emacs/emacs.html) is a free powerful editor available for many platforms and operating systems. See http://www.gnu.org/software/emacs/windows/ntemacs.html for a Windows 95/98/ME, and 2000 version of Emacs. Xemacs (http://www.xemacs.org/) is based on GNU Emacs with full GUI support.

The package VHDL-mode adds support for VHDL editing to GNU Emacs or XEmacs. It includes the following features:

- Syntax highlighting
- Indentation
- Template insertion (electrification)
- Insertion of file headers
- Insertion of user-specified models
- Port translation / test bench generation
- Sensitivity list updating
- File browser
- Design hierarchy browser
- Source file compilation (syntax analysis)
- Code hiding
- Word/keyword completion
- Block commenting
- Code fixing/alignment/beautification
- Postscript printing
- VHDL'87/'93 and VHDL-AMS supported
- Comprehensive menu
- Fully customizable

VHDL-mode is maintained by Reto Zimmermann and Rod Whitby.

URL: http://opensource.ethz.ch/emacs/vhdl-mode.html

VIM

Description: VIM is a free clone of the UNIX standard text editor Vi. It's available for many platforms and operating systems and can handle VHDL syntax (via a special VHDL package included in the distribution).

URL: http://www.vim.org/

NEdit

Description: NEdit is a reely-distributable GUI style plain-text editor for X/Motif systems. It is very easy to use, especially for those familiar with the Macintosh or MS Windows style of interface. NEdit supports syntax highlighting with built-in patterns for VHDL, Verilog, and more.
Pre-built, tested executables are available for Silicon Graphics, Sun (Solaris & SunOS), HP, Digital Unix, Ultrix, IBM AIX, Linux, and VMS systems.

URL: http://nedit.org

GRASP

Description: The GRASP Project has successfully created and prototyped a new algorithmic level graphical representation for software: the Control Structure Diagram (CSD). The primary impetus for creation of the CSD was to improve the comprehension efficiency of Ada source code and, as a result, improve software reliability and reduce software costs. Since its creation, the CSD has been expanded and adapted to include other languages. GRASP provides the capability to generate CSD's from Ada 95, C, C++, Java and VHDL source code in both a reverse and forward engineering mode with a level of flexibility suitable for professional application.

GRASP is available for Unix (SPARC SunOS, SPARC Solaris, SGI Irix, X86 Linux, IBM AIX, DEC Alpha (Digital UNIX and Linux), Power MachTen 4.1) and for Win95/NT.

URL: http://eng.auburn.edu/grasp/

Prism Editor

Description:

The Prism Editor is an 'environmentally friendly' shareware editor designed for Windows NT/95/98. It has a lot of features like code formatting, color syntax highlighting, column editing, block commenting/uncommenting. Currently it supports VHDL, Verilog and ABEL and any custom language. Further, VHDL HLP (see Section 1.5) may be used to add context sensitive help to the editor.

URL: http://www.iol.ie/~dmurray/Prism/Prism_Editor.html

e93

Description: e93 is a portable window open sourced based text editor oriented to the needs of programmers. It was begun in 1993 (thus the name). It uses the mouse, selections, cut/copy/paste, and closely follows the model of editors on the Macintosh and NeXT platforms. e93 is highly configurable and supports user-configurable syntax highlighting (including VHDL, C/C++, JAVA). Binaries are available for Linux and Windows.

URL: http://www.e93.org/

jEdit

Description: jEdit is a programmer's text editor written in Java and released under the terms of the GPL. Some of jEdit's features include syntax highlighting for 70 languages,

built-in macro language (BeanShell), auto-indenting of source code, folding (indent and 'marker' based), unlimited undo/redo, extensible plugin architecture, with more than 50 plugins available.

URL: http://www.jedit.org/

1.4 Text Tools

MVP (Make VHDL Pretty)

Description: MVP is a free VHDL pretty printer using FLEX and C. It can produce ascii or postscript. FLEX generated C code is included. Contributed by Paul Elliott. MVP is available as an improved version MVP v2.6 (Martin Gumm).

URL: http://c3iwww.epfl.ch/people/martin/gumm.html

A version v1.1.1 (based on MVP v1.1) updated for USA A size paper and assoaciated font bugs is available at
URL: http://vhdl.org/vi/vhdlsynth/mvp_v1_1_1.tar.gz
URL: ftp://vhdl.org/pub/vhdlsynth/mvp_v1_1_1.tar.gz

Another version v1.3.3 (based on previous versions from P.S. Elliot and M. Gumm) by N.J.H.M. van Beurden can be downloaded from
URL: http://www.djnickmanns.cjb.net/
URL: http://djnickmanns.webjump.com/

MVPx (GUI frontend to MVP)

Description: MVPx is a front-end for the MVP (Make VHDL Pretty) program.

Contact: Nick van Beurden, djnickmanns@email.com

URL: http://www.djnickmanns.cjb.net/
URL: http://djnickmanns.webjump.com/

vhdl-nice

Description: Another VHDL "Pretty Printer" called "vhdl-nice" from Michael Knieser.

Contact: Michael Knieser, Email: knieser@alpha.ces.cwru.edu

There are differnt version for VHDL 1076/87 and VHDL 1076/93 available

- VHDL 1076/87
  URL: http://bear.ces.cwru.edu/tools.html
- VHDL 1076/93
  URL: http://bear.ces.cwru.edu/tools.html

VHDL -> mif Pretty Printer Perl Script

URL: ftp://ftp.estec.esa.nl/pub/vhdl/tools/prog2mif

A VHDL-1076.1 (AMS) Parser/Pretty-Printer written in SWI_Prolog

(see Section 1.1)

a2ps

Description: a2ps is an Any to PostScript filter. It started as a Text to PostScript converter, with pretty printing features and all the expected features from this kind of programs. But today, style sheets to convert C, C++, TeX, VHDL, ... source files to PostScript are available as well.

URL: http://www-inf.enst.fr/~demaille/a2ps/

1.5 Miscellaneous

VHDL Validation Suite

Description: VHDL VALIDATION SUITE RELEASE ANNOUNCEMENT from Oct 15th, 1990:
The VHDL Validation Suite, which was developed at Va. Tech with funding provided by CAD Language Systems Inc., Daisy/Cadnetix, Genrad, MCC, Silicon Compiler Systems, Vantage Analysis, and Zycad is now ready for public release. The suite contains 2295 tests which cover 100% of the 1865 test points defined for the VHDL Language Reference Manual.

Contact: Professor J. R. Armstrong, Bradley Department of Electrical Engineering, Virginia Tech, Blacksburg, VA. 24061-0111, phone: (540) 231-4723, fax: (540) 231-3362, Email: jra@vt.edu
URL: ftp://digres3.visc.vt.edu/pub/suite/vpi.tar

See also FAQ Part 1, Section 4.4.

VESTs

Description: Models from the Billowitch test suite as well as models from the figures in Peter Ashenden’s books "The Designer’s Guide to VHDL" are available under the GNU Public License in a test suite titled VESTs.

URL: ftp://ftp.ececs.uc.edu:/pub/users/paw/software/vests.tgz.

VHDL Makefile Maker and Source Code Splitter

Description: vmkr is a vendor independent makefile generator for VHDL. vsplit is a tool that splits up VHDL source code so that there is only one design unit per file, a requirement for vmkr to work properly.

URL: http://tech-www.informatik.uni-hamburg.de/vhdl/vhdl.html.

vhdl-2-c: A VHDL to C conversion tools

URL: http://bear.ces.cwru.edu/tools.html
Files: vhdl2c-bins-0.1.tar.gz (binaries) and vhdl-2-c_source-0.1.tar.gz (source)

vhdlprof - A VHDL profiling tool

URL: http://bear.ces.cwru.edu/tools.html
Files: vhdlprof-bins-0.1.tar.gz (binaries) and vhdlprof_source-0.1.tar.gz (source)

vhdl2html: A VHDL to HTML converter

Description: Re-formats and colorizes your VHDL into HTML for viewing and printing.

Contact: Jon Connell:jco@egnetz.uebemc.siemens.de
URL: http://bear.ces.cwru.edu/tools.html
URL: ftp://alpha.ces.cwru.edu/pub/VHDL/contrib/vhdl2html.tar.gz

hdl2html: A perl script which converts VHDL or Verilog to HTML

This PERL script takes an HDL file (VHDL or Verilog) and produces a HTML formatted version of it. The Verilog mode is not as well tested as VHDL mode. It has been run on NT but not on Unix.

URL: http://www.papillonresearch.com/

Verilog -> VHDL translator

Description: The Verilog -> VHDL translator is only tested on DEC C++.

URL: ftp://ic.berkeley.edu/pub/Tools/verilog2vhdl.tar.Z

A DATABASE SERVER OF PUBLIC DOMAIN VHDL MODELS

Description: More than 42 Mbytes of VHDL related material are available. According to Usenet group comp.lang.vhdl, VHDL examples, models and related matters are still hard to find, we have started gathering as many VHDL models as possible, and have decided (when reading the news) that the resulting database could be of great help for other potential users.
Authors: Yannick HERVE/Francois PECHEUX (rigidly shortened by T. Dettmer)

Contribution are welcommed in /incoming (management by herve@erm1.u-strasbg.fr) Suggestions and encouragments at herve@erm1.u-strasbg.fr.
The database structure and contents are:

- /pub/vhdl/00README.first To be read first
- /pub/vhdl/ISCAS.vhdl/ 63 ISCAS benchmark translated in VHDL
- /pub/vhdl/misc/ FAQs, IEEE recommendations
- /pub/vhdl/models.vhdl/ with one subdirectory per model
- /pub/vhdl/packages.vhdl/
- /pub/vhdl/papers/ Interesting papers or electronic books
- /pub/vhdl/results.at.ERM-MACAO/
- /pub/vhdl/synthese.models.vhdl/
- /pub/vhdl/tests.for.vhdl/ Tests and comments
- /pub/vhdl/utils.for.vhdl/ VHDL grammars, tools, and C related files

Contact: Email: herve@erm1.u-strasbg.fr
URL: ftp://erm1.u-strasbg.fr/pub/vhdl/
URL: http://erm1.u-strasbg.fr/db/

V2C: VHDL to C translator

Description: v2c is a tool that automatically translates a VHDL source into an equivalent C program, i.e. a C function with the same input-output behavior of the digital circuit the VHDL represents. v2c can cope with data-flow and behavioral architectures, sequential or combinatorial, with most of the sequential and concurrent statements supported.

Contact: Cristian Ghezzi, Email: http://www.ghezzi.net/contact/index.htm
URL: http://www.ghezzi.net/pro/v2c/index.htm

IDaSS

Description: IDaSS is an Interactive Design and Simulation System for digital circuits, targeted towards VLSI and ULSI designs of complex data processing hardware. IDaSS describes a design as a tree-like hierarchy of schematics. The design files can be converted into different hardware description languages (like VHDL or Verilog). Some further features of IDaSS are the integration of design and simulation via a build in simulator (not VHDL simulation) and the capability to generate test vector files.

Contact: Email: A.C.Verschueren@ele.tue.nl
URL: http://www.ics.ele.tue.nl/~ad/idass.html

FMF Free Model Foundation

Description: The Free Model Foundation (FMF) is a not for profit organization. It has been created to promote the development and free distribution of simulation and analysis models of electronic components. It is the Foundation's belief that the utility of these models will be maximized by distributing them as unencrypted source code. The FMF website has VHDL models and timing files for over 1000 common components available for free download as well as various papers and style guides related to component modeling.

FMF provides:

- Models
- Modeling services
- Model distribution
- Backannotation tools
- Educational services

Contact: Email: rick.munden@vhdl.org
URL: http://vhdl.org/fmf

VHDL-GUI

Description: VHDL-GUI is a free graphical tool for capturing, drawing, editing, and navigating hierarchical block-diagrams, and for producing corresponding structural VHDL code. The VGUI tool is easy to learn-and-use, with a style based on popular web-browser, word-processor/drawing tools. It accommodates arbitrarily complex multi-level diagrams, while providing WYSIWYG hardcopy printouts. VGUI produces IEEE-1076 standard VHDL code. It is not vendor-specific and can be used with any VHDL compiler/simulator tools.

Contact: Email: chein@atl.lmco.com
URL: http://www.atl.external.lmco.com/rassp/vgui/index.html

VHDL HLP

Description: VHDL HLP is a free Windows based VHDL help file. VHDL HLP may be used to add context sensitive help to the Prism Editor (see Section 1.3).

Contact: Email: dmurray@iol.ie
URL: http://www.iol.ie/~dmurray/Prism/VHDL_Help.html

KPP - A VHDL Pre-Processor

Description: KPP is a pre-processor, similar to CPP, for VHDL applications. It provides many standard functions such as #def, #undef, #ifdef, #include, etc. It also provides for loops and some other features. The program will run on Win95, Win98, and WinNT. Authored by Ingrid Brill.

URL: http://rk.gsfc.nasa.gov/richcontent/Software_Content/KPP.htm

OpenTech CDROM

Description: The aim of this project is to compile open hardware designs and free design tools and put them on distribution CDROM to be available for all hardware designers.

URL: http://www.opencores.org/OIPC/projects/OpenTech/

The TimingAnalyzer Program

Description: The TimingAnalyzer can be used to draw and edit timing diagrams and check for timing problems in digital systems. The diagrams can be included in word processing documents, printed, and saved as JPG or GIF image files. The signal diagrams are saved as text files so they are easy to modify or distribute.
Currently, the tool is free while it is in beta testing.

URL: http://www.timinganalyzer.net/

TimingTool

Description: TimingTool allows engineers to graphically edit timing diagrams and then save the diagram in TDML format. The saved TDML can then be translated into Verilog / VHDL.

URL: http://www.timingtool.com

ABEL/Altera HDL (AHDL) to VHDL converter

Description: The free ISE WebPACK software from Xilinx includes a HDL converter to translate ABEL or Altera HDL (AHDL; do not confuse it with Analog VHDL which is also somtimes denoted as AHDL) designs to VHDL.

URL: http://www.xilinx.com/

ChipVault

Description: ChipVault is a VHDL/Verilog Chip Design organization tool. A (incomplete) list of its features is

- Automatically sorting and displaying design files hierarchically. Designed to handle multi-million gate designs with hundreds of RTL files.
- Provides a Fast and Simple mechanism for navigating design hierarchy and launching favorite editors and tools (compile,lint,etc.) on design files.
- Simple to use Revision Control system for archiving file changes and Group Development, keeping ’Mainline’ syntax-free versions of files separate from the minute-to-minute alterations. Prevents multiple designers from working on the same file simultaneously.

URL: http://chipvault.sourceforge.net/

2. Companies and their Products/Services

This section lists companies and their products/services related to VHDL. If you notice that some informations are not up-to-date please send a note to the editor.

Further, the "ISD Magazine" at http://www.isdmag.com and the "Programmable Logic Jump Station" at http://www.optimagic.com are good web sources for informations on EDA tools.

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Accolade Design Automation, Inc.
550 Kirkland Way, Suite 200
Kirkland, WA 98033
USA
(425) 828-2122, (800) 470-2686
(425) 739-2163 FAX
http://www.acc-eda.com
Email: info@acc-eda.com
WWW: http://www.acc-eda.com
Japan Distributor:
InterLink, Inc.
1-5-21-1325 Mori Isogo-Ku
Yokohama 235 JAPAN
Phone: 81-45-40-28220
Accolade Design Automation, Inc. develops and markets high-performance
tools for VHDL and FPGA users. Products include a Microsoft Windows
(3.1, ‘95 and NT compatible) VHDL simulator in Personal and Professional
editions. The PeakVHDL simulator uses direct-compile technology, and
includes a source code browser, integrated ’make’ facilities, and
integrated source file editor. The PeakFPGA synthesis product integrates
directly with PeakVHDL to provide a combined simulation and synthesis
environment for popular FPGA devices including Xilinx, Altera, Actel,
Lattice, Lucent and AMD. The Accolade Design Automation Web Site
http://www.acc-eda.com includes a free Introduction to VHDL
tutorial. Evaluation software is available, as is a textbook titled
"VHDL Made Easy!". Call or email for special low-cost educational
programs and packages.
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Aldec, Inc.
Corporate Headquarters
2230 Corporate Circle
Henderson, NV 89014
USA
Tel: (702) 990-4400
Toll Free: (800) 487-8743
Fax: (702) 990-4414
email: sales@aldec.com
web: www.aldec.com

Aldec, Inc., an 18-year EDA tool provider, is committed to delivering
high-performance, HDL-based design verification software for UNIX,
Linux and Windows platforms. Aldec is dedicated and responsive to
serving its customers’ needs. It is recognized that to be productive
in today’s market and to best serve customers in the future, new
technologies and innovations that go beyond traditional methods of
conducting business in the EDA industry must be pursued. Aldec is
committed to customer service and is actively developing a company
that will evolve along with its customers’ designs.
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Alternative System Concepts, Inc.
PO Box 128 Windham NH 03087
tel (603) 437-2234 fax (603) 437-2722
Email: info@ascinc.com
WWW: http://www.ascinc.com

verilog2vhdl : verilog2vhdl translates hierarchical Verilog HDL to VHDL by using an HDL object kernel which converts the input to an intermediate format and then back to the other HDL. It makes a full translation of structural Verilog, and a partial translation of behavioral Verilog. It supports all synthesizable Verilog as a subset and uses a combination of IEEE and tool-specific VHDL packages to perform the translation. VHDL that is created by verilog2vhdl is functionally equivalent to input Verilog, and because of one-to-one mapping of Verilog to VHDL, output VHDL is easy to understand. Comments are preserved and placed after the line in the translated code most closely matching the design intent. Test benches can be translated also to verify that the output is correct. Output VHDL is IEEE 1076-1993 compliant. Node-locked and floating licenses are available for HP-UX, Solaris, SunOS and Windows NT platforms.

VHDL2verilog: VHDL2verilog translates hierarchical VHDL (full structural, part RTL) to Verilog HDL. Verilog that is created by VHDL2verilog is functionally equivalent to input VHDL. Comments are preserved and placed after the line in the translated code most closely matching the design intent. Test benches can be translated also to verify that the output is correct. Both IEEE Std 1076-1993 or IEEE Std 1076-1987 compliant VHDLs are processed by the system and output Verilog is compatible with any Verilog-XL compatible simulator. Node-locked and floating licenses are available for HP-UX, Solaris, SunOS and Windows NT platforms.

VBIT®: JTAG Test Synthesis for ASIC and IC Designers. VBIT®, which was the industry’s first RT level JTAG Test Synthesis tool, is available directly from the developer ASC. The product features automatic boundary scan test logic insertion synthesis by a tool using technology independent IEEE 1149.1 macros to read VHDL or Verilog input and produce corresponding RT Level VHDL or Verilog output. A Simulation Testbench is created in Verilog or VHDL to test the Boundary Scan Circuitry. A BSDL output file is also created for easy interface to Board Level ATE and creating test vectors. VBIT® also supports custom mapping to vendor-specific JTAG cell libraries and custom interfaces for internal scan, memory and logic BIST. VBIT® frees engineers from learning the tedious details of IEEE 1149.1 standard and manually inserting boundary scan test logic into their ASIC, IC or MCM designs in an error-free rapid way. VBIT® scan implementation at the RT level promotes design re-use. Tools that insert boundary scan test at the gate level are used too late in the design cycle to be truly technology independent. Furthermore, by implementing boundary scan before logic synthesis, the designers can synthesize functional core logic and test logic concurrently and avoid timing and area violations in the entire chip. This saves costly design iterations. Node-locked and floating licenses are available for HP-UX, Solaris, and SunOS platforms.

FRITS: FRITS is an object-oriented framework to interface with other EDA tools and facilitate rapid development. FRITS translates Verilog

HDL or VHDL descriptions into an intermediate format (common object format) and stores the data in an object kernel in memory. The object kernel is accessible to the EDA tool developer via an Application Program Interface (API). FRITS also provides an elegant mechanism for easy extraction of the stored design data. All operations by FRITS are fast.

****

Associated Professional Systems (APS)
3003 Latrobe Court
Abingdon, Maryland 21009
USA
Phone: 410-515-3883
Fax: 410-661-2760
Email: eda@associatedpro.com

APS develops FPGA test boards and packages them with EDA software at very low prices. The APS-X84 XILINX Foundation Kits offer VHDL Schematic capture, simulator, ABEL HDL, XACT router, and VHDL multimedia

tutorial plus the X84 ISA FPGA test utility board for prices as low as $650.00. The kit comes with VHDL examples and C code to control and download to the FPGA board from either the supplied XCHECKER cable or from the PC ISA bus.

Check out the details at http://www.associatedpro.com/.

These deals can’t be beat!

****

Cadence Design Systems, Inc.
HDL Design Group
270 Billerica Road
Chelmsford MA 01824
508-667-8811
OR
555 River Oaks Pkwy.
San Jose, Calif. 951134
Eileen Elam (Public relations representative)
(408) 943-1234
Germany:
Mr. Grothe
phone: 02236 68051 seems now: 02236/962130 (Vertrieb)

- Leapfrog - Full IEEE 1076 Simulation Environment Using Native Compiled Code
- Synergy - VHDL and Verilog Logic Synthesis and Optimization
- Verilog-XL - Verilog HDL and accelerated gate simulator
- NCSim - native-compiled Verilog and VHDL simulation in the same kernel: completely unified mixed-language simulation kernel supporting VHDL 93, etc.
- Envisia Ambit - VHDL & Verilog, high-capacity synthesis
- Envisia PKS - Ambit synthesis with knowledge of the physical (layout) dimension
- Affirma FormalCheck - Model checking of VHDL and Verilog designs
- Affirma Heck - Equivalence checking of VHDL & Verilog designs
- Affirma HAL - HDL Analysis and Lint tool for both VHDL and Verilog

Valid (part of CADENCE now)
2820 Orchard Pkwy.
San Jose, Calif. 95134
Germany:

Muenchen,
phone: 089/710050 seems now: 089/570960 (Applikation)
 compiler, simulator
 Now sells Intermetrics tools

www: http://www.cadence.com/
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Cypress Semiconductor
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San Jose, California 95134, U.S.A
Phone: (408) 943-2600
Fax : (408) 943-2741
- Information is also available from any of our sales offices Worldwide -
Warp2: Warp2 is a state-of-the-art VHDL compiler for designing with
Cypress PROMs and PLDs. Warp2 utilizes a proper subset
of IEEE 1076 VHDL as its Hardware Description Language (HDL) for its design
entry. Warp2 accepts VHDL input, synthesizes and optimizes the entered
design, and outputs an industry standard JEDEC map for the desired device.
This JEDEC file may then be simulated with the Cypress NOVA simulator
(included in Warp2).
Warp2 is available on PC(Windows) and Sun platforms.

www: http://www.cypress.com/
****
Dolphin Integration
BP   65, ZIRST
39, avenue du Granier,
38242 MEYLAN, FRANCE.

Tel : +33 (0)4 76 41 10 96
Fax: +33 (0)4 76 90 29 65

WWW: http://www.dolphin.fr

Email: solution@dolphin.fr

Product:

SMASH (TM) is a mixed-signal multi-level simulator for ASICs, systems
and PCBs. SMASH can simulate circuits with parts described in SPICE
format, parts in Verilog-HDL, parts in VHDL, and parts in VHDL-AMS.
SMASH also supports true analog behavioral modeling in ABCD (based on
C language). Complex systems, built using ’silicon IP’ delivered in
various formats, can be described most efficiently using the right
level of modeling and abstraction for each part. SMASH is a single-
process tool, and does not suffer from the complexity issues associated
with backplane solutions.
It delivers unprecedented performance for mixed-signal simulation based
on standard formats.
SMASH is available on Windows 9x/NT/2000, and also on Sun Solaris
machines. It is interfaced with popular schematic entry packages, such
as Cohesion Chip Designer. Evaluation versions (functional but limited
to small circuits) are available from the Web site
(http://www.dolphin.fr/medal/smash/smash_overview.html)
and also numerous application notes. Call or email for special
conditions applicable to educational use.
****

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WWW : http://www.doulos.com

Having built a formidable reputation for high quality, application based VHDL, Verilog® and SystemC training, Doulos continues to develop courses and project services for engineers pushing the boundaries of new technology and methodologies. Doulos is independent of tool and technology vendors, so all course attendees can learn using the tools of their choice. Public courses are run across Europe, in the UK, France, Germany and The Netherlands, and customised onsite courses can be delivered worldwide.

Courses available (duration in days in brackets):

Foundation Level: (Preparatory training for design environment)

Essential Digital Design Techniques (2)
Essential Perl (3)
Essential Tcl/Tk (coming soon)
PaceMaker multi-media CBT (Verilog or VHDL, self teach)

Standard Level: (Beginner to full project readiness)

Introduction to VHDL: A Foundation for PLD or ASIC design (2)
Further VHDL: Essential training for a PLD or ASIC design project (3)
Comprehensive VHDL: The above two modules together (5)

Comprehensive Verilog : Beginner to full PLD/ASIC project readiness (4)

Introduction to C/C++ for Hardware Engineers: enough C/C++ to understand SystemC, or other C-based design tools (2)
SystemC : Use of SystemC for design and modelling (3)
Comprehensive SystemC : The above two modules together (5)

VHDL-AMS Workshop: Introduction to VHDL-AMS (2)

Expert Level: (Advanced design and verification techniques)

Expert VHDL Design: Writing for Advanced Synthesis and Re-use (2)
Expert VHDL Verification: Advanced testbenches/modelling using VHDL (3)
Expert VHDL: The above two modules together (5)

Expert Verilog Design: Writing for Advanced Synthesis and Re-use (2)
Expert Verilog Verification: Advanced testbenches/modelling using VHDL (3)
Expert Verilog: The above two modules together (5)

Xilinx TechClass: Using VHDL with Xilinx Architectures (2 or 3)
Altera TechClass: Using VHDL with Altera Architectures (2)

Course Materials

Comprehensive, fully indexed course notes (ideal as a reference manual).
Workbook packed with exercises (50% of the course is hands-on).
Doulos Golden Reference Guide (language, syntax, semantics, tips).
Tool Tour guides (to support your choice of tools and technologies).
Multi-media CD-ROM (an optional course preparation and refresher aid).

Publications

VHDL Pacemaker: multimedia VHDL tutorial on CD-ROM
HDL Pacemaker: multimedia Verilog tutorial on CD-ROM
VHDL and Verilog Golden Reference Guides

Partner companies

Doulos has associate companies in France, Germany and The Netherlands (SystemC courses only). Courses may be delivered in English, French, or German.

France

Francois Durif
AmbLot SARL
166 Boulevard du Montparnasse
F-75014
Paris, France
Tel : +33 (0)1 42795748
Fax : +33 (0)142795747
http://www.amblot.com

Germany

Gerhard Wagner
Mikroelektronik Akademie
Garbsener Landstrasse 10
Hannover 30419
Germany
Tel : +49 (0) 511 277 1970
Fax: +49 (0) 511 277 1699
http://www.meak.de

The Netherlands (SystemC courses only)

Clemens Stemerdink
Signa Technology
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7550 AZ Hengelo (0)
The Netherlands
Tel: + 31 74 2555 699
Fax: + 31 74 2555 698
http://www.signa-tech.nl
DS Diagonal Systems AG
Tumigerstr. 71
CH-8606 Greifensee
Switzerland

Phone +41 1 905 60 60
Fax +41 1 905 60 69
WWW: http://www.diagonal.com/
E-mail (from all countries): info@diagonal.ch

Products:
BestBench is a VHDL testbench design- and analysis-tool that allows
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an earlier stage of the design process.
Unlike the manual and tedious testbench design, BestBench automates
the process by creating self-checking, reactive and stand-alone VHDL
testbenches.
BestBench is available for Solaris, SunOS, HP-UX and Windows NT.

WAVE-Link provides a bidirectional link from your simulation environment
to the HP16500 Logic Analyzer. It enables the design engineers to
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to compare the response data measured by the HP16500 with the expected
simulation data.
WAVE-Link is available for SunOS and HP-UX.

BestLink/81200 allows to reuse VCD simulation data directly in the
HP81200 data generator/analyzer platform.
BestLink/81200 is available for Solaris, SunOS and HP-UX..
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EASICS, the VHDL Design Company.
Easics is an independent ASIC design company and offers a variety of
services related to the design of digital ASICs. These services
include the design of ASICs (up to a testable netlist) and FPGAs
(including prototyping), VHDL-based design consulting and ASIC design
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Easics has a track record of ASIC designs in telecommunications (ATM,
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For more information, look at our WWW-site http://www.easics.com/
or contact Dirk Callaerts, Marketing Manager (dirk@easics.be),
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Tel +32-16-395 604, Fax +32-16-395 619
****
Esperan
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SN8 2RB
United Kingdom

Tel: +44 (0)1672 520101
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Exemplar Logic

Exemplar Logic pioneered the approach of applying logic synthesis techniques to FPGA design. Today, it continues to develop and market logic synthesis software, as well as, other design automation tools for the high-level design (HLD) solution for FPGA, CPLD, and ASIC devices. Exemplar Logic’s software products offer customer improved time-to-market, reduce development costs, and enhanced product quality. Supported platforms include UNIX (HP, Sun) platforms in server and non-server environments, Windows NT, Windows 95, and Windows 98. Employees hail from semiconductor and EDA companies, with specific expertise in software tools research and development, manufacturing, marketing, and sales.

Visit the Exemplar Logic website (http://www.exemplar.com) for more information or contact:

Exemplar Logic, Inc.
880 Ridder Park Drive
San Jose, CA 95131
1-800-632-3742
+44 1276 28899
info@exemplar.com

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Frontier Design

Frontier Design offers design, analysis and implementation tools, reusable cores and design services to developers of leading edge telecommunication, consumer and multimedia products. The company has developed state-of-the-art algorithm compiler technology and has acquired unique application expertise to meet the demanding design requirements in today’s products.

The A|RT product line is an exciting family of products from Frontier Design. A|RT stands for Algorithm-to-RT (register transfer) and embodies Frontier’s unique Algorithm-to-Silicon design methodology. The A|RT products allow driving the HDL-based hardware design process directly from a C-code specification of the algorithm. This significantly reduces the design-time that is required to move algorithms into ASIC and FPGA implementations!

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Visit Frontier Design's Website at http://www.frontierd.com or contact info@frontierd.com for more information.

Contacts:
 USA:
  Frontier Design Inc
  100 Rialto Place, Suite 815
  Melbourne FL 32901 - USA
  Tel: +1.407.728.7750
  Fax: +1.407.728.9670

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  Abdijstraat 34
  3001 Heverlee
  Belgium
  Tel: +32.16.39.14.11
  Fax: +32.16.40.60.76

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FTL Systems, Inc.
Contact: 924 Sierra Lane NE
Rochester, MN 55906
products@ftlsys.com
Main Number: +1 507 288 3154
Web: http://www.ftlsystems.com

Distributors available in North America and Japan (see WWW for details)

Products:
VHDL Complete OEM Analyzer/Elaborator (Fall 1996 Release)
VHDL Optimizing Compiler/Simulator (Early 1997 Release)
Other VHDL and Verilog products coming soon...

Public Service: VHDL-93, VHDL-AMS Validation Suite (1997 Release)

Glad to meet you at:
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US DAC
ASP DAC
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Full Circuit Ltd
Chippenham
UK
Phone: +44 1249 720161
Fax: +44 7020 966228
Email: sales@fullcircuit.com
WWW: http://www.fullcircuit.com

VHDL Test Bench Tool

A tool to generate test benches that is both low-cost and unlike other tools not constraining. Price 1/1/2001 is GBP80, $120 approx.

The tool generates fully functional VHDL but VHDL simple enough for hand editing to be used to expand its functionality without limit. The actual complex test vectors are stored in a separate file. Plus, to make use of this flexibility, the test vectors can include variables (e.g. integers, times, etc.) in addition to the UUT input and output signals.

Complex signal relationships can easily be defined and again are not constrained to a fixed set of constructs. This includes loops and loops within loops. The loop counter can be used in the definition of the signals. The test bench can be modular and individual modules checked separately. A graphical plot of the test bench can be displayed which is especially useful when looping is used.

A limited demo version is available and 30 day trial unlimited licenses available by using the form.

Screenshots, worked example, downloads and license requests:
http://www.fullcircuit.com/TBtool.htm

The Test Bench tool program requires Excel 97+ so PC or MAC. No knowledge of Excel is required.

In addition Full Circuit can provide bespoke VHDL IP, digital design, analog design, and software. The web site also has some useful freeware for PC (not VHDL related).

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Green Mountain Computing Systems, Inc.
83 River Road Apt. C
Essex Junction, VT 05452
Email: support@gmvhdl.com
WWW: http://www.gmvhdl.com/

Products
Green Mountain VHDL Compiler, Professional Edition This professional-level IEEE VHDL simulator based on direct compile technology provides fast simulation and advanced debugging features. Currently available for Linux only (Windows version to be released).

Green Mountain VHDL Compiler, Educational Edition This edition provides a lost-cost solution to VHDL beginners while providing full support for the most commonly used features of VHDL. Currently available for DOS and Linux.

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I-LOGIX
3 Riverside Drive
Andover, MA 01810
Tel. 978-682-2100
Fax. 978-682-5995

Statemate MAGNUM, a graphical behavioral modeling tool allows hardware engineers to design with the precise graphical language of STATECHARTS- a powerful extension of state transition diagrams. Designers can create behavioral and functional models of

circuits, analyze the design using the simulation and dynamic
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Email: info@interhdl.com
Ftp site: http://ftp.interhdl.com
Web page: http://www.interhdl.com
V to VH: Verilog to VHDL translator. Converts Verilog designs into
  equivalent VHDL designs. Covers about 95% of the language including
  the full structural and synthesizable subsets. The output VHDL code is
  semantically and synthesis-wise equivalent to Verilog source, and is
  very readable.
V to VL: VHDL to Verilog translator. Converts VHDL designs into
  equivalent Verilog designs. Covers about 95% of the language including
  the full structural and synthesizable subsets. The output Verilog code
  is semantically and synthesis-wise equivalent to VHDL source, and is
  very readable. Translation include generate statements, enumerations,
  aggregate constants, etc. Comments are being preserved in the output
  code.
****
JRS Research Laboratories Inc.
 2300 East Katella Ave., Suite 300
 Anaheim, CA 92806-6048
 Telephone (714) 704-1670
 FAX (714) 704-1675
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Fax: +1 919-479-1671
WWW: http://www.mench.com
Mr. Menchini is an independent EDA Consultant with over seventeen years
of industrial EDA experience, specializing in the hardware description
languages VHDL and Verilog, and in high-level design methodologies.
He offers training, custom code and model development, and marketing
and technology consulting to EDA companies and users. His current and
former clients include Chrysalis Symbolic Design, DEC, Ikos, Research
Triangle Institute, Rosemount Aerospace, Synopsys, Tellabs, Thinking
Machines, TSSI, VHDL International, Viewlogic, and Zycad.

Mr. Menchini, who holds Bachelor’s and Master’s degrees from Stanford University, is a member of IEEE (Senior Member), CS, ACM, IFIP Working Group 10.2, and the Association for Automated Reasoning.

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MCC Microelectronics and Computer Technology Corp.
3500 West Balcones Center Dr.
Austin, Texas 78759
USA
Phone: +1 (512) 338 3598
e-mail: ask@mcc.com
 simulator

www: http://www.mcc.com/

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Model Technology Incorporated
8905 S.W. Nimbus Ave, Suite 150
Beaverton, OR. 97008-7100 USA

Model Technology is the market leader in VHDL according to Dataquest based on units and revenue. V-System is considered the most popular VHDL simulator with over 11,000 revenue units sold worldwide and is available on Workstation (HP, SUN Solaris, SUNOS5, and RS600) and PC (x86 and Pentium based Windows 3.1, 95, and NT).

Model Technology sells a full line of HDL solutions for VHDL, Verilog, and Mixed HDL simulation.

V-System is sold direct through Value-Added Resellers and through OEM relationships such as Mentor Graphics, Exemplar, Data-I/O and Escalade.

For more product information as well as who to contact: please visit our home page at http://www.model.com, email us at sales@model.com, or call us at 1-503-641-1340

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Mentor Graphics
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070-7777
for System-1076 and QuickVHDL
  contact: Brian Caslis (brian_caslis@mentorg.com)
  phone: hone: (503)685-1404 Fax: (503)685-1268
  WWW: http://www.mentor.com/
for VHDLsim
  contact: John Harris (john_harris@mentog.com)
  phone: 503-685-4735
Germany:
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phone: 0211/591011
Fully integrated compiler/simulator/debugger design development system:
  System-1076 - QuickSim-II based VHDL. Source-level debugger, supporting
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                Design(TM) environment - available now.
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            integrated within the GDT design environment, and
            supports the use of VHDL models with analog and M models in
            the same design.
  AutoLogic VHDL - VHDL synthesis
  VHDLNet - netlist schematics into VHDL structural description

```
  Design Architect - VHDL oriented text editor (and schematic editor)
  QuickVHDL - Full IEEE 1076 Simulation Environment using Direct-Compiled
            Code Technology. Includes integration with Design Architect
            for entry and AutoLogic VHDL for synthesis. Available September
            1993
**********************************************************************
Papillon Research Corp. - Specialists in Hardware Engineering
142-Q North Rd.
Sudbury, MA 01776

ph: 978-371-9115
fax: 978-371-9175
Email: info@papillonresearch.com
WWW: http://www.papillonresearch.com

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Dept. of Electrical Engineering
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Univ. of Pitsburgh, 15261
Email: vhdl@ee.pitt.edu
see anonymous ftp: ee.pitt.edu (130.49.15.1) in pub/vhdl-info for files
README, letter.txt, license.PS, assurance.PS ...
not public domain, but 150$
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Productivity Engineering
Gesellschaft fuer Prozessintegration mbH
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D-71083 Herrenberg

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Productivity Engineering is offering training, consulting-services and
software for quality and productivity enhancements within the process
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access to 15 experienced specialists in the area electronic design
automation, engineering data management and product data management.

Productivity Engineering is a neutral and independent service-company,
providing professional consulting and high-tech products.

Electronic Design Automation
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Services provided within the EDA-Market are Turn-Key-Designs, Project-Coaching, Hardware-Design, Library-Development for synthesis & simulation as well as dataconversion tools and services for pcb-databases to convert between leading eda-tool-suppliers. Running VHDL- and Verilog-Design-Seminars on a regular basis in cooperation with Doulos provides an actual overview of available design-technologies as well as flexibility in using different design-environments.

Methodology training

Through a long cooperation with DOULOS (since 1993) we supply full range of DOULOS-VHDL and Verilog methodology training in central Europe, which could be adapted to the application areas of our customers. These trainings classes are tool independent; different design tools within one course are offered on a regular basis to enhance experience. With the four and five-days-classes a multimedia CD-ROM for preparantion and as a reference is supplied. Technology guides offer a short introduction to backend FPGA-tools as well as an introduction to FPGA architectures and coding for these FPGA architectures. The workshops focus on the stuff presented so far and show the application with practical examples developed by experienced designers.

Application Support

Within the application support we help our customers through HDL-Coding-Standards, HDL-Code-Reviews and Design-Flow-Optimization. HDL-Coding-Standards are of importance when emphasizing design reuse through HDL-code reuse or when porting HDL-code to different technologies or different simulators or synthesis tools.

We offer feasability studies and cost-analysis for FPGA- and ASIC-Design-projects.

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Starting from specification we implement our customers product with a turn-key-approach with fixed pricing. We even work out the specification verbally or as a behavioural model of the design in colaboration with our customer. Our consultants join your project teams and strengthen your knowledge and enhancing the design capacity of your company. We offer flexible add-on-resources for RTL-coding as well as Testbench-Development.

During our projects you will get into touch with our technical management, thus enhancing the effectivness of our work through short responses to your requirements.

We employ specialists, with great experience caused by consultancy project within the large american and german semiconductors. We have application know how in Multimedia, PCI-bus-systems and PCMCIA.

Productivity Engineering succeeded in automotive application projects
as well as space- and air-industry and telecommunications.
****

Qualis Design Corpration
PO Box 4444
Beaverton, OR, USA, 97075-4444
(503) 531-0377 fax: (503) 629-5525
Email: info@qualis.com
WWW: http://www.qualis.com

Overview
  Qualis Design Corp of Beaverton, OR, offers high quality expert
  consulting services in all aspects of using HDLs (both VHDL and
  Verilog) including training, design environment, code management,
  tooling, tool integration, behavioral modeling, test planning,
  testbench infrastructure, testcase implementation, synthesis,
  gate-level verification and more...

Training
  Our classes differ from the traditional bottom-up, gate-to-behavioral
  HDL training approach and reverses the flow starting with high-level
  descriptions, testbench and top-down methodology. We feel this
  high-level approach to training better fits an advanced design process
  encouraging students to learn a methodology, and not just a
  language. More than 70% of the time is spent on hands-on exercises
  using the latest version of state-of-the-art VHDL, Verilog and
  synthesis systems.

        High-Level Design Using VHDL   (5 days)
        High-Level Design Using Verilog   (5 days)
        Advanced Techniques Using VHDL   (3 days)
        Advanced Techniques Using Verilog   (3 days)

Products
  VHDL language Quick Reference Card   pub/qrcs
  1164-based packages Quick Reference Card   pub/qrcs
  Verilog language Quick Reference Card   pub/qrcs
  Makefile generator for VHDL models   pub/vhdl/vmk
****

Sandstrom Engineering
3611 Vista Drive
Manhattan Beach, CA 90266-3245
voice   310.545.7108
email   johan@sandstrom.org
fax   310.546.7396
website http://www.sandstrom.org

PreSynth.vhd supplements simulation by analyzing your RTL code.
It checks for nonsense constructs, the dreaded "reset problem",
non-synthesizable constructs, and performs hundreds of
lint-type checks. It also permits you to use an expanded subset
of VHDL, which PreSynth.vhd converts to synthesizable VHDL.

Consulting available.
****

Saros Technology Ltd.
Business and Technology Centre
Stevenage

Herts
SG1 2DX
United Kingdom
Phone : ++44 (0)1438 746433
FAX: ++44 (0)1438 310093
Email : 100135.1052@compuserve.com
Contact : Chris Rose
Products :
Saros Technology Ltd. Specialise in the provision of a complete range of VHDL development tools for the PC and Workstation platforms. As the sole UK distributor for Model Technology, Exemlar Logic and Translogic products we offer design entry, simulation and synthesis tools for FPGA and ASIC design.
Saros Technology have also developed and offer a VHDL context sensitive editor for the PC under Windows. VHDL Turbo Writer comprises the powerful Codewright Editor from Premia corp, providing a fully featured, multi window, multi document text editor with line numbers and colour coding. This is enhanced by a rich set of VHDL templates, integration with the Model Technology VHDL compiler and full error detection within the editor environment.

Price L495 with volume discounts for 5 or more.
****
SEE Technologies see Summit Design.
****
Seeds VHDL ENvironment (SVEN)
Seed Solutions, Inc.
7505 Sherman Road
Chesterland, OH 44026
216-729-7500
Commercial parser
****
Semantic Designs, Inc.
12636 Research Blvd #C214
Austin, Texas 78759
USA
Phone: 512-250-1018
Fax: 512-250-1191
Email: info@semdesigns.com

Semantic Designs provides software tools for automating the analysis/modification/synthesis of large scale specifications in many languages, including VHDL and Verilog.

In particular, the DMS Reengineering Toolkit (http://www.semdesigns.com/Products/DMS/DMSToolkit.html) can parse arbitrary languages, automatically build compiler-like Abstract Syntax Trees (ASTs), carry out analyses and surface-syntax transforms on ASTs, and prettyprint the ASTs back to source language form, for specifications of up to 2 million lines.

This tool is ideal for constructing custom analyzers and/or synthesizers. Since DMS handle multiple languages (including C/C++, Java, Ada, ...), and can have custom languages easily added as well, it would be ideally suited as the foundation for CoDesign applications.

www: http://www.semdesigns.com
****

Seodu Logic, Inc.
http://www.seodu.co.kr
MyCAD PC based Toolset and Environment for VHDL Simulation, Synthesis etc.
****

SICAN GmbH
Garbsener Landstr. 10
39419 Hannover
Phone: +49-511/277-1491
Fax: +49-511/277-2490
Email: info@sican.de
WWW: http://www.sican.de

USA:
SICAN Microelectronics Corp.
400 Oyster Point Blvd., Suite 512
So San Francisco, CA 94080
Phone: +81-650 871-1494
Fax: +81-650 871-1504
WWW: http://www.sican-micro.com
Email: info@sican-micro.com

Company Overview SICAN is a microelectronic design and technology licensing company, specializing in communications, digital signal processing, multimedia and networking applications. We provide our targeted markets with leading edge design solutions by combining state-of-the-art Design Methodology with highly optimized Core Technology.

VHDL Products Digital Design Services In the recent five years we have completed over 200 Digital VHDL-Designs including synthesis. You can participate in our VHDL Design Experience by realizing Turnkey Projects with us or by hiring our experienced engineers as a Consultant or as a Designer in one of your inhouse projects. In addition, you can order Training Services (VHDL, VerilogHDL, Synthesis etc.) presented by our highly experienced Senior Engineers.

DesignObjects™ SICAN's DesignObjects™ give design teams a new alternative. Now, it is possible to buy synthesizable, technology independant cores (VHDL and/or VerilogHDL) to quickly integrate standards-based functionality required in a design.

DesignObjects™ from SICAN encompass a broad spectrum of technologies:
* Audio Decoders (e. g.MPEG-2 Layer 1&2 + Dolby AC-3 5.1 Channels)
* Broadband Access Functions (e. g. QAM-Demodulator)
* Bus Interfaces (e. g. PCI, USB, IEEE1394, CAN Bus Controler, IIC Master / Slave Interface)
* Cryptographic Functions (e. g. DVB Descrambler)
* Digital Photography (e. g. JPEG Video Decoder with Color Space)
* General Purpose Microcontroller (e. g. 8051 Microcontroller)
* Industrial Functions (e. g. Motor Control Module, Pulse Width Modulation)
* Multimedia Accelerators (e. g. Video Conferencing Hybrid Accelerator)
* RAM Interfaces (e. g. SDRAM Timing Generator)
* Telecommunication/Communication/ATM (e. g. UTOPIA Interface)
* Video Decoders (e. g. MPEG-2 Video Decoder with Letterbox Features)

* Video Encoders (e. g. MPEG-1 Video Encoder)
* Video Processors (e. g. PAL/NTSC Video Encoder Interface)

DesignObjects™ can be delivered as an all-inclusive assembly of netlist or RTL source code, technical specifications, test benches, synthesis scripts and application support.

Any further questions? Don’t hesitate to contact us at:
Phone +49-511/277-1491
or visit our web-page http://www.sican.de

****

Silicon System Solutions P/L
2/12 Wattle Valley Road
Canterbury Victoria 3126, Australia
Phone: +61 3 9888 4774
Fax: +61 3 9888 4224
Email: info@silicon-systems.com
WWW: http://www.silicon-systems.com

Products and services
* VHDL Cores (IP)
  Fast-track to your system integration, with a selection of Synthesis and Simulation Cores tuned to fit your needs.
* FPGA and ASIC design consultants
  Our design experts are ready to help you with CPLD/FPGA and ASIC development. Specify the models you require, and use our design experts as a dedicated resource in your project development.
* ED4W-HDL - Powerful HDL Editor for VHDL and Verilog
  ED4W-HDL is a VHDL/Verilog Editor for WindowsNT/95 and Windows 3.1. HDL extensions developed by ASIC/FPGA Designers at SSS, for ASIC/FPGA Designers. A very effective productivity tool.

****

SoftSmiths Pty. Ltd.
54 Wylma St.
Holland Pk. 4121
Australia
Phone: + 61 7 847 2990
Fax: + 61 7 847 2707
Email: info@softsmiths.oz.au
Products: VHDL Design Entry schematiX11-VHDL
An X11 Sun based VHDL design entry package for the purpose of capturing VHDL designs in a graphical format and writing VHDL netlist descriptions. Being in a graphical form it is much simpler to transfer the design concepts to other colleagues and maintain the design over the life time of the product.
Allows direct access to and editing of the functional code for any block at any level in the design hierarchy. Interfaces with any third party VHDL simulator.
Cost effective site licences allow UNIX based productivity at prices per user comparable to PC based products.
freely licenced copies of SoftSmiths’ VHDLcapture tools are available for anonymous ftp download from ftp.tmx.com.au /cust/softsmiths/
Educational Licence Restrictions apply, if you are in doubt ask us first (info@softsmiths.oz.au). If you are a commercial site you may download this software for evaluation purposes.

www: http://www.webventures.com.au/ElectTech/softsmiths/

****
Summit Design, Inc.
9305 S.W. Gemini Drive
Beaverton, OR 97005-7158
USA
Telephone: 503-643-9281
FAX: 503-646-4954
Contact: (various)
Product Name: Visual HDL

Visual HDL[TM] integrates four graphical languages, a textual language, a simulator and debugger, and code generators for VHDL and Verilog. It uses a state-of-the-art, object-oriented user interface, featuring a graphical design browser.

Visual HDL includes intelligent editors for input of block diagrams, state diagrams, flowcharts, and truth tables, besides VHDL text. This comprehensive set of languages helps you to work at any level of abstraction, and to mix levels of abstraction.

With Visual HDL you can create a high level description of your design and validate it by execution. An event-driven, interactive simulator works in tandem with a source-level debugger for rapid analysis of the system. While the simulator runs, you can set breakpoints, modify existing signals and variables, single-step through multiple execution threads, and trace various activities. Visual feedback appears on your source descriptions, in the windows of their editors, for easy tracing.

Following design verification, Visual HDL generates VHDL or Verilog code customized for the commercial synthesis tool you specify.

Visual HDL is available for UNIX and for Microsoft Windows.

www: http://www.summit-design.com/
****
SynaptiCAD Inc.
520 Prices Fork Rd #C4
Blacksburg, VA 24060
USA
Phone: (540)953-3390 or (800)804-7073
Fax: (540)953-3078,
Email: sales@syncad.com
WWW: http://www.syncad.com

VHDL Test Bench and Stimulus Generators

SynaptiCAD develops stimulus generators and test bench generators for VHDL. SynaptiCAD’s premier product TestBencher Pro, is a self-testing multi-diagram test bench generator. TestBencher Pro can detect glitches, bad logic levels, and violations of setup and hold times in simulation output. Users draw inputs to a simulation and specify expected simulation outputs using graphical constructs called samples. TestBencher Pro generates VHDL test benches with extra code which verifies that graphically-specified conditions are met by a simulator’s output. Users can concatenate timing diagrams together to mimic a series of read/write bus cycles. TestBencher Pro also has looping and conditional constructs that enable simulation results to control what stimulus is applied next.

SynaptiCAD also offers WaveFormer Pro, a timing diagram editor and VHDL stimulus generator. Users draw a timing diagram that represents the input to a simulation. Then the user exports the timing data as a VHDL

process that contains either transport or wait statements. WaveFormer Pro supports all VHDL data types. Even user defined types like "type MyColor is (RED, BLUE, GREEN)" can be exported with both type and state information. TestBencher Pro and WaveFormer Pro are offer three different ways to enter signal waveforms: (1) a graphical environment for drawing, (2) text based temporal equations, and (3) boolean equations of other signals. Other simulator formats are also supported including Verilog, SPICE, Viewlogic, Orcad, Mentor QuickSim, HP Logic Analyzers, HP Pattern Generators, and more, so timing diagrams can be reused at different times during design process.

For a FREE evaluation of WaveFormer Pro or TestBencher Pro, product info, and pricing, check out our web site: http://www.syncad.com/

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Synopsys Inc.
USA
Synopsys, Inc.
700 East Middlefield Road
Mountain View, California 94043-4033 U.S.A.
Phone: (415)962-5000
FAX: (415)965-8637
Germany (moved)
Synopsys, GmbH
Stefan George Ring 2
D-8000 Muenchen 81   Germany
Phone: 89/9939120
FAX: 89/99391217
URL: http://www.synopsys.com/
Products:
 Design Compiler - Constraint-Driven Logic Optimization (CMOS & GaAs)
 VHDL Compiler - VHDL Logic Synthesis
 HDL Compiler - Verilog HDL Synthesis
 Test Compiler - Test Synthesis (Auto. Test insertion + ATPG)
 VHDL System Simulator - 100% language compatible VHDL behavioral simulation
 Cyclone - A cycle based VHDL simulator

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Translogic

Translogic BV
Keesomstraat 17
P.O. Box 620
6710 BP EDE
The Netherlands
Phone: +31 (0)318 642076
Fax: +31 (0)318 641761

Translogic USA Corp.
341 Tres Pinos Road
Suite #202B, CA
95023, Hollister
USA
Phone: 831-636-4664
Fax: 831-636-4625

e-mail: info@translogiccorp.com
web site: http://www.translogiccorp.com/

Products:

EASE/HDL: Easy to use graphical HDL entry tool. Generates VHDL and Verilog output for both simulation and synthesis purposes. Featuring hierarchy browsing and state machine diagrams. Reverse engineering, automatically generating graphical blocks for inclusion in block diagrams.
EALE/HDL: Language-sensitive text editor, featuring color coding, undo/redo, multi-document edit, keyword templates, synthesis templates, completely customizable user interface and an extensive

on-line help. Supports VDHL, Verilog, ABEL, C, as well as synthesis
script languages.

Products available on both PC and UNIX systems. For more information
or a free evaluation copy please visit our web site:
http://www.translogiccorp.com.
****

Topdown Design Solutions, Inc.
71 Spit Brook Road, Suite 301
Nashua, NH 03060
Phone: (603) 888-8811
Fax: (603) 888-7694
contact: Frank Hrobak or Art Pisani
Products:
   VHDL SelfStart_Kit - a self-paced tutorial to learn VHDL quickly and
     easily,
   VBAK/XILINX - An Xilinx XNF to VHDL translation, which allows VHDL
     simulation of both pre- and post-layout designs, including full-timing
     simulation models.
   Universal DRAM VHDL source code model
   QuickStart, QuickStart2+1 - VHDL education at your site!
   Model Technology V-System VHDL Simulator - on PC/Windows and UNIX
     platforms
   Consulting + Custom Training services available, including VIP (VHDL
     Insertion Program) as well as public training.

www: http://www.topdown.com/
****

TransEDA, Inc.
Contact: Tom Borgstrom, John Molyneux
Address: 985 University Avenue, Los Gatos, CA 95032
Phone: 408-907-2000
Fax: 408-907-2085
Email: info@transeda.com
Web: http://www.transeda.com
Products:
  Verification Navigator - Integrated Design Verification Environment
    VN-Cover - Verilog and VHDL Code Coverage
    VN-Check - Parametric Design Rule Checker for Verilog and VHDL
    VN-Optimize - Test Suite Analysis & Optimization
    VN-State - FSM Extraction and Coverage
    VN-Activity - Circuit Activity Analysis

  VN-Check - Stand alone Verilog and VHDL parametric design rule checker

  State Navigator - Comprehensive FSM Debug and Verification Environment
****

Valid see CADENCE (part of)
****

Vanilla CAD Tools, Inc.
Rt. 4, Box 146
Saluda, SC 29138-9126   USA
803-445-7227
Email: vanilla@emeraldis.com
Vanilla VHDL is a complete implementation of the 1987 IEEE standard,
including configurations. Like the old MCC system, it is completely
text-based, with a gdb-like command set for its debugger/simulator.
Unlike MCC, it does not translate to C, but instead uses an interpreted

engine, since this simplifies debugger implementation and enhances
portability.
To fund further development of the tools, they are now commercially
available on the PC. A 386 or better is required. An introductory
price is in effect until July 30, 1995.
****
Vantage Analysis Systems, Inc. (purchased by Viewlogic)
USA:
  42808 Christy Street, Suite 200
  Fremont, CA 94538
  phone: +1(510) 659-0901 fax: (510) 659-0129
  contact: John Willey
Europe:
UK:
  Grove Court Business Centre
  Hatfield Road
  Slough
  Berkshire SL1 1QU (UK)
France:
  Daniel Langois
  MISIL Design
  2 Rue De La Couture Silic 301
  94588 Rungis Cedex (France)
Sweden:
  Lars Lindqvist :- Engineer
  Hardi Electronics
  P.O. Box 966
  Varvadersvagen 4P
  S-220 09 Lund (Sweden)
  Phone +46 46 117790
Germany:
  Klenzestrasse 11
  8045 Ismaning b. Muenchen
  089/99652217
Japan:
  Okura & Co, Ltd
  3-6 Ginza, 2 chome
  Chuo-ku, Tokyo 104 (JAPAN)
  phone: 011-81-3-566-6000, fax: 011-81-3-563-5447
Vantage Spreadsheet, 100% IEEE 1076 VHDL Source Code Debugger Concurrent
Compiler Network License
Integrated VHDL Schematics/Simulator Read/Write Mentor/Valid/EDIF Schematics
Logic Automation & ASIC libraries Hardware Modeler On Sun & HP machines
and Silicon Graphics, Apollo
****
VAutomation Inc.
20 Trafalgar Square
Suite 443
Nashua, NH USA 03063
TEL:(603)882-2282 FAX:(603)882-1587
Email: info@VAutomation.com
Contact: Eric Ryherd
Supplier of Technology Independent Synthesizable VHDL Models
  Models of complex functions such as 8-16 bit
  Microprocessors and their peripherals.

www: http://www.vautomation.com
****

VeriBest, Incorporated
USA:
6101 Lookout Road
Boulder, Colorado 80301
Phone: 303.581.2300
Fax: 303.581.9972
toll free: 800.VERIBEST
WWW: http://www.veribest.com
Email: info@veribest.com
United Kingdom:
44.1793.511199
Germany:
49.89.96284.0
France:
33.1.41.76.35.00
Nordic:
46.8.92.54.00
Asia/Pacific:
852.2.893.3621
Japan:
81.3.3797.5277

Company:
VeriBest, Inc. is a broad line supplier of EDA solutions that enable companies to solve their critical business issues by doing more and spending less. VeriBest pioneered the Windows NT EDA market by introducing its VeriBest PCB design solution in 1994 and continues to offer the best EDA price/performance available in the industry.

VHDL Products:
VeriBest Graphical High-Level Design: VeriBest Graphical High-Level Design is a language independent, graphical, state-machine entry and debug environment. VBGHLD includes a state table editor, a state diagram editor and a state flow graph editor. VBGHLD is integrated with VeriBest Design Capture to give you a single environment for your design definition needs. VBGHLD outputs both VHDL and Verilog.

VeriBest VHDL:
Introduced at DAC ’96, VeriBest VHDL is a VHDL 1076-93 compliant simulator offering unique debug features such as a Network Traverser. VBVHDL is an Windows NT-product and utilizes standard NT ease-of-use features such as signal drag-n-drop into the various display and debug features.

VeriBest High-Level Design:
VeriBest High-Level Design is a VHDL/Verilog synthesis application that outputs VHDL and Verilog for post-synthesis simulation and outputs data for the VeriBest Design Optimizer.
****
VhdlCohen Training, Consulting, and Verification
* On Site Training for Synthesis, Testbench Designs, and design processes.
* On-site or e-commerce Consultant
  Build Verification and Testbench Models in VHDL
  RTL Design per Your Requirements
  Code Reviews to Ensure Compliance to Requirements
  (e.g., functional, readability, reusability, synthesizability,
  completeness).
  EDA Tool evaluation

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-----------------------------------------------------
VhdlCohen Training, Consulting, Verification
Ben Cohen vhdlcohen@aol.com  (310) 721-4830
http://www.vhdlcohen.com/
Author of following textbooks:
VHDL Coding Styles and Methodologies, 2nd Edition,
  isbn 0-7923-8474-1 Kluwer Academic Publishers, 1999
VHDL Answers to Frequently Asked Questions, 2nd Edition,
  isbn 0-7923-8115-7 Kluwer Academic Publishers, 1998
*****************************************************************
VHDL Technology Group
  100 Brodhead Road, Suite 140
  Bethlehem, PA 18017
  Tel: 610-882-3130 Fax: 610-882-3133
  Email: sales@vhdl.com
VitalGen(tm) v1.0, a high-end model generator , produces Vital 3.0
  compliant models.
Sledgehammer: A language aware editor for VHDL, VERILOG, C and C++
  developers. Runs under Microsoft Windows, Windows-NT and Windows-95.
  Provides language specific keyword identification and template
  expansion, keyword color coding, auto-indentation and multi-file
  search & replace, to name a few of the many features. Priced
  comparable to most PC office automation software.
Std_DevelopersKit: A collection of four packages:
(1) Std_IOpak: includes routines for text I/O
    testbench development, and type conversions.
(2) Std_Mempak: routines which you can use to develop memory models.
    SRAMs, DRAMS, ROMS, and VRAMs.
(3) Std_Regpak/Synth_Regpak: provides synthesizable datapath subprograms
(4) Std_Timing: provides routines to model device
    timing and delays. Complements the VITAL packages.
Used by over 1000 engineers worldwide.
Supports: All major simulators.

www: http://www.vhdl.com/
*****************************************************************
Viewlogic Systems Inc.
293 Boston Post Road West
Marlboro, MA 01752
phone: 508/480-0881 or 1-800-422-4660, FAX: 508/480-0882, TELEX 174242
Germany:
Viewlogic Systems GmbH
Muenchner Str. 12
85744 Muenchen-Unterfoehring
phone (49)-89-9572490 FAX (49)-89-95724949
Powerview - open framework based on CFI
 ViewSim/VHDL: simulator (behavioural and structural)
 ViewSynthesis, Silcsyn and ViewArchitect: FPGA, ASIC
 and behavioural synthesis
 Viewgen: schematic drawing synthesis (indirectly coupled to EDIF)
 Export.1076: Automatic VHDL netlist generation from Viewlogic schematic
    (which accepts EDIF)
 ViewFSM: graphical behavioral modeling tool that allows you to draw
    statecharts and automatically produce VHDL for simulation and
    VHDL that is optimized for synthesis
*****************************************************************
Vista Technologies, Inc.
USA:
```

1100 Woodfield Road, Suite 437
Schaumburg, IL 60173-5121
Phone: (708) 706-9300, fax: (708) 706-9317
contact: David Jakopac
Email: hdlinfo@vistatech.com

Japan:
Marubeni Hytech Corp.
Marubeni Hytech Bldg.
20-22, Koishikawa 4-Chome
Bunkyo-ku, Tokyo 112
JAPAN
Phone: 81-3-3817-4871, Fax: 81-3-3817-4880
Contact: Ken Sakamaki

Europe:
LEDA S.A.
Europarc, Bat. C
F-13013 Marseille
FRANCE
Phone: 33+ 91 06 26 73, Fax: 33+ 91 06 24 66
Contact: Olivier Thibault

All of Vista's tools generate VHDL suitable for simulation, with optional generation specifically for synthesis. All of Vista's tools allow users to import VHDL Packages so that custom types, functions and procedures can be utilized.

StateVision: Graphical state machine editor. Generates VHDL from bubble diagrams of concurrent state-machines for simulation or synthesis. Open and customizable system. Can be integrated with off-the-shelf VHDL simulators for a complete design and debug environment (set breakpoints in states, step with animation, etc.) Shipping 4Q94.

DesignVision: Graphical behavior modeling editor. Uses the DesignVision methodology ("threads") for specifying behavior graphically. Generates VHDL for simulation or synthesis. Open and customizable system. Users can customize the generated VHDL to their own style and build their own graphical primitives (including how the primitives generate VHDL). Can be integrated with off-the-shelf VHDL simulators for a complete design and debug environment (set breakpoints in threads, step with animation, etc.) Special introductory price through Oct. '94. Shipping now.

Vista Model Creator: Spreadsheet-like interface that generates VHDL from function and state machine tables for simulation or synthesis. Compact representation ideal for ALUs, instruction decoders, etc. Shipping now.

VHDL Language Assistant: Syntax-directed editor with built-in knowledge of VHDL. Not just language templates, full VHDL-1076 built-in. No special representation: can read, edit and write any VHDL file. Shipping now.

The VHDL Developer: Suite of tools that includes VHDL Language Assistant and Source Code Library Manager. Shipping now.

The VHDL Developer Plus: Suite of tools that includes Vista Model Creator, VHDL Language Assistant, and Source Code Library Manager. Shipping now.

****

Vital, Inc.
4109 Candlewyck Drive
Plano, TX 75024
U.S.A

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Ph:  +1 (214) 491-6907 Fax: +1 (214) 491-6909
Email:  info@vital.com or owner-crisp-list@uunet.uu.net
CRiSP is a graphical file editor on various UNIX and Windows platforms,
  which combines the power and  flexibility of other editors such as
  vi, or Emacs but in a user-friendly fashion.
  CRiSPs' dynamic syntax coloring for VHDL adds a new dimension to
  the coding cycle. You can print the VHDL code in color too !!.
  The editor comes with advanced template editing for VHDL, and
  has an extensible macro language to customize it to the users
  environment.
**********************************************************************
VIZEF Limited
The Old Coach House
Adwell
Thame
OXON
Tel: 44 (0)1844 281066
Fax: 44 (0)1844 281070
Email: steve@vizef.demon.co.uk

SpeedSim high speed cycle simulation for fast verification of RTL
Verilog. Typically 10-100 times faster than Verilog-XL.

Virtual-ICE, for co-verification of hardware and firmware. This tool
enables ASIC/Software designers to run their firmware with the RTL level
ASIC and a CPU/DSP core(s) of choice. Using this tool allows you to
start final firmware debug and software performance analysis before a
physical device (FPGA or engineering samples) is available.

FlowHDL graphical tool for RTL design and testbench capture using the
ASM methodology. VHDL and Verilog output targeted for user specified
synthesis environment. Design environment supports multiple interacting
state machines, data path specification, multiple clock domains,
sync/async reset specification, synthesis directives and much more.
**********************************************************************
Walnut Creek CDROM
  4041 Pike Lane, Suite E
  Concord, CA  94520
  800/786-9907 or 510/674-0783
  FAX 510/674-0821
  Email info@cdrom.com
        ADA CDROM has (besides other stuff)
        uc      -- the University of Cincinnati VHDL repository
        VHDL (VHSIC Hardware Description Language)
     Vhdl Mailing list moved to vhdl-sw@ece.uc.edu.  All messages to the
     list will be automatically archived on ftp.ece.uc.edu.
     These messages are located in /pub/mailing-lists/vhdl-sw directory.
     ftp Archive moved to thor.ece.uc.edu
     Eventually, the ftp archive will be moved to ftp.ece.uc.edu too.
     NEW SUBSCRIPTIONS SHOULD BE SENT TO listserver@ece.uc.edu. THE BODY
     OF THE MESSAGE SHOULD BE AS FOLLOWS: subscribe vhdl-sw Your-name
**********************************************************************
X-Tek Engineering
X-HDL, Verilog to VHDL translator. X-HDL has the power to perform 100%
translation of your synthesizable Verilog code to VHDL. Also X-HDL
can translate non-synthesizable constructs such as delay statements
and display statements, with additional support coming in the near future.
X-HDL has an intuitive, X-Windows based user interface.
```

```
DEMO VERSIONS OF X-HDL FOR SUN AND HP PLATFORMS ARE NOW AVAILABLE
VIA http://www.x-tekcorp.com/download.htm
For additional information, send your request to:
thomasr@mail.msen.com

www: http://www.x-tekcorp.com/
*********************************************************************
Zycad Corporation
  (ZyCads VHDL SOFTware was sold to Synopsys)
47100 Bayside Parkway
Fremont, CA 94538-9942
USA
phone: 1(510)623-4400
fax: 1(510)623-4550
  VIP VHDL Instruction Processor
  hardware accelerators
*********************************************************************
```

3. VHDL Compilers for PC's

The following lists are (probably) incomplete. Therefore, if you have any additional information or find any errors or compiler missing: please send me a note. If you have good or bad experiences with this tools (particularly with free software) please let me know. Thanks for all corrections.

Further, the "ISD Magazine" at http://www.isdmag.com and the "Programmable Logic Jump Station" at http://www.optimagic.com are good web sources for information on EDA tools.

3.1 Free Compiler

A project to develop a free (under the Gnu Public License (GPL)) VHDL-93 compliant compiler/simulator has started. If you want some further information check out the "FreeHDL" home page at http://www.freehdl.seul.org/.

Here is a list of (more or less) free available compilers:

- **VHDL-AMS (Analog and Mixed Signal) simulator SEAMS**
  - Website: http://www.ececs.uc.edu/~dpl/
  - Product: Analog and Mixed Signal VHDL-AMS simulator "SEAMS".
  - Versions: Linux ... ?
  - Misc: Also available is a graphical user interface for VHDL-AMS simulation and a Spice-to-VHDL-AMS translator "SPAMS".
- **University Pierre et Marie Curie**
  - Ftpsite ftp://ftp-asim.lip6.fr/pub/alliance/
  - Website: http://www-asim.lip6.fr/alliance/
  - Product: ALLIANCE 3.2
  - Versions: Linux
    The compiler supports a subset of the IEEE 1076 VHDL standard.
  - Misc: ALLIANCE 3.2 is a complete set of CAD tools for teaching Digital CMOS VLSI Design in Universities. It includes VHDL compiler and simulator, logic synthesis tools, automatic place and route, etc...
- **VDT + INSPIRE (Seoul National University, Design Automation Laboratory)**
  - Ftpsite: ftp://poppy.snu.ac.kr/pub/vhdl/
  - Website: http://poppy.snu.ac.kr/
  - Products: VDT (VHDL Developer's Toolkitf) + INSPIRE (a VHDL Simulation Environment with **IN**cremental Analysis/Elaboration, **SP**ecialized Functions, and Incremental Waveform **RE**generation). Both packages are needed.
  - Versions: Precompiled for Linux, SUN, Windows.
    The simulation system supports a subset of the IEEE 1076 VHDL standard.
- **Vanilla Cad Tools, Inc.**
  - Website: http://www.freehdl.seul.org/vvhdlt_1.tgz
  - Products: Vanilla Cad VHDL System
  - Versions: Linux, Win95, WinNT. Note, only the Linux version is licensed free of

charge (see README.linux for further information)!
    - Misc: Supports IEEE 1076-1987 and some featuers of 1076-1993. (Remark from the editor: at least the Linux version does not have a graphical waveform viewer; however, a perl script written by Parag Birmiwal to convert simulation output data into *text* waveforms is available from http://paragb.tripod.com/wav.tgz)
- **SAVANT**
    - Ftpsite: ftp://ftp.ececs.uc.edu/pub/users/dmartin/
    - Website: http://www.ececs.uc.edu/~paw/savant (alternative download site: http://www.cliftonlabs.com/savant/download/)
    - Product: SAVANT, TyVis and warped
    - Versions: Linux, Solaris, source
    - Misc: In conjunction with TyVis and warped, Savant provides end to end parallel and sequential simulation of VHDL ’93. The Savant analyzer has been designed to easily allow the insertion of new back-ends into the tool. Further, users may modify, distribute, and use the software contained in the SAVANT software package under the terms of the "GNU LIBRARY GENERAL PUBLIC LICENSE". Binaries for Linux and Solaris 2.6 are available.
- **SIMEC GmbH & Co KG**
    - Website: http://www.hamster-ams.com/
    - Product: hAMSter
    - Versions: Win
    - Misc: hAMSter is a stand alone VHDL-AMS Simulation Environment for PCs. hAMSter supports behavioral modeling of mixed analog-digital and multi physics systems. For a limited time hAMSter can be obtained for free from the website!
- **Symphony EDA**
    - Website: http://www.symphonyeda.com/
    - Products: VHDL Simili
    - Versions: Linux, Win95/98, WinNT 4.0
    - Misc: VHDL 93 compliant (with a few exceptions) command-line compiler/simulator. The simulator supports Vital 95 (IEEE 1076.4) and SDF 2.1 and includes accelerated version of various packages (e.g. std_logic_1164). A commercial GUI version is also available.

3.2 Commercial Compiler

The commercial compilers are divided into three price categories:

Price category	Range (USD)
A	$1 < $200
B	$200 < $1000
C	above $1000

- **Accolade Design Automation, Inc.**
  - Website: http://www.acc-eda.com/
  - Product: PeakVHDL Simulator
  - Versions: Win95, WinNT, Win3.11
    Support for IEEE 1076-1987 and 1076-1993
  - Misc: Synthesis tool also available. Demo version available.
  - Price category: B
- **Aldec, Inc.**
  - Website: http://www.aldec.com/
  - Product: Active VHDL, Riviera
  - Versions: Win98, Win2000, WinNT, SUN Solaris (Riviera only), Linux (Riviera only)
    IEEE 1076-93 VHDL language-compliant. An evaluation version is available.
  - Price category: C
- **Blue Pacific Computing, Inc.**
  - Website: http://www.bluepc.com/
  - Product: BlueHDL VHDL and BlueWave
  - Versions: Linux, Win95, Win98, WinNT
    BlueHDL is a low-cost VHDL tool suite that consists of a VHDL compiler, a simulation engine and the BlueWave GUI. A free limited student version is available.
  - Price category: ?
- **Cypress Semiconductor Corporation**
  - Website: http://www.cypress.com/
  - Product: Warp2
  - Versions: Win3.1x, Win95, WinNT
  - Misc: Synthesis supports all Cypress Programmable Logic Devices. Only functional simulation.
  - Price category: A
- **Dolphin Integration**
  - Website: http://www.dolphin.fr/
  - Product: SMASH
  - Versions: Win95, Win98, WinNT, SUN. Linux/Solaris
  - Misc: SMASH is a mixed signal, multi-level simulator. It handles both analog, continuous signals, and discrete digital signals. SMASH handles functional and behavioral levels, for both analog and digital worlds. It uses SPICE syntax for analog descriptions, Verilog-HDL and VHDL for digital, VHDL-AMS and ABCD (a combination of SPICE and C) for analog behavioral, and C for DSP algorithms.
  - Price category: C
- **FTL Systems, Inc**
  - Website: http://www.ftlsystems.com/
  - Products: Exploration, Pathway, Centauri
  - Versions: AIX, HPUX, Solaris, Linux, WinNT
  - Misc: Exploration is a capacity limited low cost VHDL simulator (VHDL and

VHDL-AMS simulation with SPICE and Verilog support). Pathway is a single processor compiler/simulator for commercial applications. Centauri is a multiprocessor compiler/simulator for large commercial applications. Pathway and Centauri are available for VHDL, VHDL-AMS, Verilog, and SPICE.

- Price category: A (Exploration), C (Pathway and Centauri)

- **Green Mountain Computing Systems**
  - Website: http://www.gmvhdl.com/
  - Product: Green Mountain VHDL Compiler Professional Edition, VHDL Studio
  - Versions: Linux, Win 95, WinNT, Solaris
  - Misc: Supports nearly the entire VHDL 1076-1993 standard. A evaluation version is available.
  - Price category: B (Green Mountain VHDL Compiler Professional Edition), C (VHDL Studio)
- **SIMEC GmbH & Co KG**
  - Website: http://www.hamster-ams.com/
  - Product: hAMSter
  - Versions: Win
  - Misc: hAMSter is a stand alone VHDL-AMS Simulation Environment for PCs. hAMSter supports behavioral modeling of mixed analog-digital and multi physics systems. For a limited time hAMSter can be obtained for free from the website!
  - Price category: B
- **Model Technology, Inc.**
  - Website: http://www.model.com/
  - Product: ModelSim/VHDL, ModelSim SE, ModelSim EE, ModelSim PE
  - Versions: Win95, WinNT, SUN, HP, RS6000, Linux (beta release)
    Complete IEEE VHDL 1076-1987 and -1993 standard. Evaluation version available. A ModelSim-Altera Edition can be obtained for free from Altera's website http://www.altera.com. However, the ModelSim-Altera software provides simulation performance of 25% of ModelSim EE/SE.
  - Price category: C
- **OrCAD, Inc.**
  - Website: http://www.orcad.com/
  - Product: OrCAD EXPRESS for Windows
  - Versions: Win95, WinNT
    Simulator supports a subset of the IEEE 1076-1993 VHDL standard. The package includes schematic entry and synthesis.
  - Price category: ?
- **Seodu Logic, Inc. and MyCad, Inc.**
  - Website: http://www.mycad.co.kr/
  - Product: MyVHDL Station
  - Versions: Win95, Win98, WinNT
    IEEE 1076-1987 standard. Synthesis tool also available. Free functionally limited education version as well as time limited version (full functionality) available.
  - Price category: C

- **Symphony EDA**
  - Website: http://www.symphonyeda.com/
  - Product: VHDL Simili
  - Versions: Linux, Win98, WinNT, Win2000
    IEEE 1076-93 VHDL language compliant compiler/simulator with GUI. Demo/trial version available. Command-line version is available for free.
  - Price category: A
- **Vanilla Cad Tools, Inc.**
  - Address: Vanilla Cad Tools, Inc., Route 4, Box 146, Saluda, SC 29138-9126 USA, Tel: 864-445-7227, Email: vanilla@emeraldis.com
  - Products: Vanilla Cad VHDL System
  - Versions: Linux, Win95, WinNT. Note, the Linux version is licensed free of charge (see Section 3.1).
  - Misc: Supports IEEE 1076-1987 and some featuers of 1076-1993. (Remark form the editor: At least the free Linux version does not have a graphical waveform viewer)
  - Price category: ?
- **Viewlogic Systems, Inc.**
  - Website: http://www.viewlogic.com/
  - Product: ViewSim
  - Versions: Windows
    Complete IEEE 1076 VHDL. Synthesizer also available.
  - Price category: C
- **VeriBest, Inc.**
  - Website: http://www.veribest.com/
  - Product: VB VHDL
  - Verions: WinNT
    IEEE 1076-19987 and -1993 language support. Demo version available: at the end of 30-day evaluation period, VeriBest VHDL converts to a 2,000 gate or 2,000 line capacity limit unless purchased.
  - Price category: C
- **Xilinx, Inc.**
  - Website: http://www.xilinx.com/
  - Product: Foundation Software Series
  - Versions: Win95, Win98, WinNT
    Gate-level simulation. Integrated tool set for design entry, synthesis, implementation, and simulation.
  - Price category: C?

See also Section 2. Companies and their products/services for additional information.

4. Verilog <-> VHDL Translators

4.1 Free Verilog <-> VHDL Translators

- Author: Ephrem Wu (ephrem@ic.berkeley.edu)
  - Products:
    Verilog -> VHDL translator
  - Versions: only tested on DEC C++.
  - URL: ftp://ic.berkeley.edu/pub/Tools/verilog2vhdl.tar.Z
- Author : Vincenzo Liguori - Ocean Logic Pty Ltd (oceanlogic@yahoo.com)
  - Products:
    VHDL to Verilog RTL translator. Although limited, this program correctly translated Ocen Logic's Triple DES and JPEG cores.
  - Versions: Source code.
  - URL: http://www.ocean-logic.com/downloads.htm

4.2 Commercial Verilog <-> VHDL Translators

- **Avant! Corporation**
  - Products: Nova-Trans
    Nova-Trans provides complete RTL design portability between Verilog and VHDL. Synthesizable RTL descriptions written in one language are converted to functionally equivalent designs in the other.
  - Versions: Sun, HP, Linux.
  - www: http://www.avanticorp.com/
- **Alternative System Concepts, Inc.** (see Section 2 for more information)
  - Products: verilog2vhdl
    verilog2vhdl translates Verilog HDL to VHDL (supports most synthesizable constructs, as well as a large subset of unsynthesizable behavioral constructs)
    VHDL2verilog: VHDL2verilog translates hierarchical VHDL (full structural, large subset of RTL) to Verilog HDL.
  - Versions: Sun, HP-UX, Solaris and Windows NT.
    Evaluation available to qualified companies and individuals.
  - www: http://www.ascinc.com
- **FTL Systems, Inc.**
  - Products: HDL Exchange
    HDL Exchange[tm] VHDL, VHDL-AMS, and Verilog translation tools allow the user to convert legacy SPICE designs into VHDL-AMS or facilitate transfer of designs between Verilog and VHDL.
  - Versions: AIX, Solaris, HP-UX, Linux and Windows NT.
    Time limited License version available.
  - www: http://www.ftlsys.com/
- **interHDL, Inc.** (see Section 2 for more information)
  - Products:

V to VH: Verilog to VHDL translator.
V to VL: VHDL to Verilog translator.
V to VV: Bi-directional Verilog and VHDL translator.

- Version: UNIX, Linux ?
- www: http://www.interhdl.com

- **Interra, Inc.**
  - Products:
    VHDL-Bridge: translates Verilog RTL (and gate level) to VHDL.
  - Versions: UNIX, WinNT.
  - www: http://www.interrainc.com/
- **X-Tek Engineering** (see Section 2 for more information)
  - Products:
    X-HDL: Verilog to VHDL translator.
  - Versions: HP 9000, Sun.
    Demo version avialable. Until Dec. 31st, 2000, X-Tek is offering its premiere Verilog <=> VHDL Translator, X-HDL, free to students and universities (contact Thomas Rock thomas@x-tekcorp.com for more details).
  - www: http://www.x-tekcorp.com/

5. VHDL <-> FSM/Schematic Translators

This section lists tools which support HDL code generation from block diagrams, flow charts, finite state machine (FSM) diagrams and/or truth tables. Further, programs to convert VHDL descriptions into schematics (and vice versa) are listed as well. Any additions/updates/corrections are appreciated!

5.1 Free FSM/Schematic -> VHDL Translators

See also Section 1.5.

- **VHDL-GUI**
  - Contact: chein@atl.lmco.com
  - URL: http://www.atl.external.lmco.com/rassp/vgui/index.html
  - Versions: Linux, SUN, WinNT, Win95, Win98.
    VHDL-GUI is a free graphical tool for capturing, drawing, editing, and navigating hierarchical block-diagrams, and for producing corresponding structural VHDL code. VGUI tool accommodates arbitrarily complex multi-level diagrams, while providing WYSIWYG hardcopy printouts. VGUI produces IEEE-1076 standard VHDL code. It is not vendor-specific and can be used with any VHDL compiler/simulator tools.
- **brusey20**
  - Author: Tom Mayo (tcmayo@fang.berk.net)
  - URL: http://tech-www.informatik.uni-hamburg.de/vhdl/vhdl.html
  - Versions: source code.
    This program is used to translate a state diagram into synthesizable VHDL. The state diagram may be entered with XFig, a free drawing tool. The format which brusey20 accepts is the PIC format, which may be exported by XFig. Output is at least suitable for synthesis using Exemplar's Galileo. It may also be useful for other synthesizers.
- **gEDA**
  - Contact: Ales V. Hvezda (ahvezda@geda.seul.org)
  - URL: http://www.geda.seul.org/
  - Versions: Linux, WinNT, Win98, source code.
    The gEDA project is working on producing a full GPL'd suite of Electronic Design Automation tools. These tools are used for electrical circuit design, simulation, prototyping, and production. gEDA has a VHDL-93 and VHDL AMS netlist export backend (currently only available via anonymous CVS access).

5.2 Commercial VHDL <-> FSM/Schematic Translators

- **Mentor Graphics**
  - Website: http://www.mentor.com/renoir/index.htm
  - Product: Renoir
  - Versions: SUN. HP, WinNT, Win95, Win98.
    Renior can generate Verilog and VHDL from Moore/Mealy state, flow chart, truth

table and block diagrams for FPGA, ASIC and IC. It includes interfaces to logic synthesis, digital simulation, and HW-SW co-verification tools. With HDL2Graphics you can turn HDL text, VHDL and Verilog Intellectual Property (IP) into graphical diagrams.

- **Novassoft**
  - Website: http://www.novassoft.com/
  - Product: Debussy
  - Versions: ?
    The Debussy debugging system system helps locating and isolating the reasons for Verilog and VHDL design problems through tracing, visualization, and analysis of design structure and behavior. One feature is generating logic/bubble diagrams from RTL or gate-level netlist.
- **Summit Design, Inc.**
  - Website: http://www.summit-design.com/
  - Product: Visual HDL
  - Versions: SUN, HP, AIX, WinNT, Win95.
    Visual HDL is a HDL-based tool for graphical design, verification, optimization and reuse. Its entry level supports block diagrams, flow charts, state diagrams (bubble diagrams and ASM charts) and truth tables as well as VHDL or Verilog descriptions. Visual HDL can generate block diagrams, flow charts and state diagrams from existing HDL code.
- **Tanslogic**
  - Website: http://www.translogiccorp.com/
  - Product: EASE
  - Versions: Win95, Win98, WinNT, Solaris > 2.4, HP-UX > 9.0, Linux
    EASE/HDL: Easy to use graphical HDL entry tool. Generates VHDL and Verilog output for both simulation and synthesis purposes. Featuring hierarchy browsing and state machine diagrams. Reverse engineering, automatically generating graphical blocks for inclusion in block diagrams.
- **VeriBest, Inc.**
  - Website: http://www.veribest.com/
  - Product: VeriBest Graphical High-Level Design
  - Versions: WinNT, Win95, Win98.
    VeriBest Graphical High-Level Design is a language independent, graphical, state-machine entry and debug environment. VBGHLD includes a state table editor, a state diagram editor and a state flow graph editor. VBGHLD outputs both VHDL and Verilog.
- **Visual Software Solution**
  - Website: http://www.statecad.com/
  - Product: StateCAD
  - Versions: WinNT, Win95, Win98.
    StateCAD automates the development of state machines and data flow logic. StateCAD automatically identifies logical problems such as stuck at states and reset violations. Once a design is error free, StateCAD translates it to synthesizable VHDL, Verilog, Abel, or Altera HDL.
- **Escalade (acquired by Mentor Graphics)**

- Website: http://www.escalade.com/
- Product: DesignBook
- Versions: Win, WinNT, Sun Solaris, HP HPUX.
  Escalade's DesignBook is an integrated, high-level design solution for the authoring, integration and delivery of system-on-chip (SOC) designs. DesignBook includes (besides other tools) a state machine designer, a truth table designer, a flowchart designer and imports VHDL and Verilog designs.

6. C/C++ to VHDL Translators

This section lists commercial tools which support HDL code generation from C and/or C++ source. Any additions/updates/corrections are appreciated!

- **JRS Research Laboratories Inc.**
  - Website: http://www.jrs.com/
  - Product: LegaC
  - Versions: ?
    LegaC translates an input program coded in ANSI C into an equivalent behavioral VHDL source-code program. The output program is logically equivalent to the input program in the sense that a VHDL compilation and simulation of the translated program will produce the same results as a compilation and execution of the original C source program.
- **Forte Design Systems**
  - Website: http://www.forteds.com/
  - Product: Cynthesizer
  - Versions: ?
    Cynthesizer is a tool that takes a Cynlib design (Cynlib is a set of C++ classes that provide a vocabulary for hardware modeling in C++) and produces an equivalent representation in Verilog or VHDL while maintaining the bit- and cycle-accuracy of the design. Higher-level data structures, such as C++ classes, are automatically transformed into functionally equivalent Verilog or VHDL. Other object-oriented features of C++, such as inheritance, are automatically resolved in the resulting Verilog or VHDL.
- **Frontier Design**
  - Website: http://www.frontierd.com/
  - Product: A|RT Builder
  - Versions: Win98, WinNT, Sun Solaris, HP HPUX, Linux
    With A|RT Builder a designer can automatically convert a C description into an RTL description, expressed either in VHDL or Verilog HDL. The resulting HDL code can be used directly in a logic synthesis flow, or can be further optimized using behavioral synthesis tools.

7. VHDL’93 Support of Simulator/Synthesis Tools

The following table lists the VHDL’93 support of various simulators/synthesizers. The list was compiled from postings to comp.lang.vhdl (thanks to Evan Shattock for providing the initial table). Please send additions/updates/corrections to the editor!

Vendor	Product	Version	Type	Support	Remarks
MTI	ModelSim	4.7x/5.1f/5.2x	Sim	93	
MTI	ModelSim	5.1f	Sim	93	
Cadence	Leapfrog	?	Sim	93	
Viewlogic	Speedwave	6.206	Sim	87	
Metamor	Metamor	?	Syn	93	
Synopsys	DC	?	Syn	87	’93 support announced
Synopsys	DC99		Syn	93	
Synopsys	FPGA Express	2.1.x	Syn	87+	’93 support announced
Synopsys	FPGA Express	3.4	Syn	87+	improved ’93 support
Synopsys	VSS	1998.08	Sim	93	
Exemplar	Galileo	4.2	Syn	93	
Exemplar	Leonardo	4.2.x	Syn	93	
Exemplar	Spectrum	1998.2	Syn	93	
Synplicity	Synplify	?	Syn	93	

"Type" is the type of the product:

- Sim: simulator
- Syn: synthesis tool

"Support" denotes the supported VHDL language level:

- 87: tool supports VHDL’87 only
- 87+: tool supports VHDL’87 and some VHDL’93 features
- 93: tool supports VHDL’87 and VHDL’93

See also Section 2. Companies and their products/services for additional information.

Part 4: VHDL glossary

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